REMARKS/ARGUMENTS

Claims 1-3, 5-39, 41, 42, 46 and 48-51 remain in the present application, of which claims 1, 22 and 41 are independent. None of the claims has been amended herein. Applicants respectfully request reconsideration and allowance of claims 1, 22 and 41.

Applicants thank the Examiner for the time and courtesy extended to applicants' attorney (Jun-Young Jeon, Reg. No. 43,693) during the telephone interview of October 8, 2004. During the interview, claims 1 and 2 have been discussed in reference to U.S. Patent No. 5,883,670 ("Sporer et al."). No agreement as to allowability has been reached.

I. "Response to Arguments" in the August 11, 2004 Office Action

Page 2 of the August 11, 2004 Office Action states that "[a]pplicant's arguments filed May 13, 2004 have been fully considered but they are not persuasive. As addressed below, Sporer et al. teaches the claimed limitations." In the same page, the Office Action states that "Sporer teaches the north bridge," and cites Col. 2, line 57 to Col. 3, line 21; figs. 1-2 of Sporer et al. without providing any detailed comparison.

A. Disclosure of north bridge function

While PCI Bridge 34 in FIG. 1 of Sporer et al. has a PCI bridge function, a mere PCI bridge or north bridge is not what the present application is directed to. Using an external north bridge or an external PCI bridge, such as the PCI Bridge 34 which is external to the video processing circuit 22 in FIG. 1

of Sporer et al., "increases number of chips in the system and introduces another potential source of system failure." (Specification as filed, page 184, lines 1-2).

In exemplary embodiments according to the present invention, by integrating a system bridge controller on the same integrated circuit chip as an MPEG video decoder, for example, the integrated circuit chip can provide both video processing and north bridge functions without increasing the number of chips or introducing another potential source of system failure.

Applicants cannot find in the above-referenced portions of the specification and drawings of Sporer et al., any disclosure for "[a] system on an integrated circuit chip comprising: an MPEG video decoder . . . and a system bridge controller having a north bridge function disposed between a CPU and a plurality of peripheral devices."

B. Delayed read and retry of reads by external masters

The Office Action on page 2 also states "Sporer discloses the system bridge controller supports delayed read and retry of reads by external masters," and cites Col. 6, lines 37-65 and Col. 8, lines 46-66 of Sporer et al. Applicants do not see in these cited sections of Sporer et al., any disclosure that a system bridge controller supports delayed read and retry of reads by external masters."

By way of example, in Col. 8, lines 46-66, Sporer et al. discloses that the PCI interface 100 acts as the bus master. With the PCI interface 100 in the video processing circuit 22 acting as the bus master, applicants do not understand in what

sense that Col. 6, lines 37-65 and Col. 8, lines 46-66 disclose a system bridge controller supporting delayed read and retry of reads by external masters." The last paragraph on page 2 through the first paragraph on Page 3 of the Office Action appears to describe the video processing circuit of Sporer et al., but applicants do not see how these sections are relevant to supporting "delayed read and retry of reads by external masters." Applicants respectfully request guidance from the Examiner.

II. Rejection of Claims 1-3, 5-39, 41-42, 46, and 48-51 under 35 U.S.C. § 102(e)

Claims 1-3, 5-39, 41-42, 46, and 48-51 have been rejected under 35 U.S.C. § 102(e) as allegedly being unpatentable by Sporer et al.

A. Rejection of Claim 1

In rejecting claim 1, the Office Action states "Sporer teaches a system on an integrated circuit chip comprising an MPEG video decoder for processing MPEG video data to generate video for displaying and means for displaying the video (col. 10, lines 1-29; figs. 1 and 9), a system bridge controller for coupling a CPU to a plurality of peripheral devices (figs. 1 and 3), wherein the CPU and the plurality of peripheral devices are situated externally to the integrated circuit chip (col. 3, line 54 to col. 4, line 28), and wherein the system bridge controller supports delayed read and retry of reads by external masters (col. 8, lines 46-56)."

Applicants do not understand that how these sections of the specification and drawings can be construed to disclose "[a] system on an integrated circuit chip comprising: an MPEG video decoder for processing MPEG video data to generate video for displaying; means for displaying the video; and a system bridge controller having a north bridge function disposed between a CPU and a plurality of peripheral devices for coupling the CPU to the plurality of peripheral devices" (Emphasis Added) as recited in claim 1 of the present application.

First of all, as discussed above, the PCI Bridge 34 in FIG. 1 of Sporer et al. is clearly external to the video processing circuit 22. In the Office Action, the controller 50 in FIG. 1 of Sporer et al. appears to be equated with a system bridge controller of the present invention. However, neither FIG. 1 nor FIG. 5 (which shows a detailed view of the controller 50) of Sporer et al. provides any indication that the controller 50 indeed has a north bridge function. In fact, the controller 50 requires an external PCI bridge (i.e., the PCI Bridge 34) to interface with the PCI Bus 36. If anything, Sporer et al. teaches away from the present invention by disclosing the use of an external PCI bridge, which results in an increased number of chips as well as providing an additional potential source of system failure.

Further, as discussed above in reference to the "Response to Arguments," applicants do not see any disclosure "wherein the system bridge controller supports delayed read and retry of reads by external masters" in Col. 8, lines 46-56 or in any other section of Sporer et al.

In more detail, according to the present invention, the system bridge controller on the same integrated circuit chip as video processing circuitry has a system bridge function and is able to support delayed read and retry of reads by bus masters that are coupled to the bus and are external to the integrated circuit chip. On the other hand, Sporer et al. in FIG. 1 discloses that the PCI bridge 34 is external to the integrated circuit chip. Further, applicants do not see any disclosure in Sporer et al. that the PCI bridge 34 supports delayed read and retry of reads by external PCI bus masters.

Since Sporer et al. does not disclose all of the features of claim 1, claim 1 is not anticipated by Sporer et al.

Further, it is not obvious at all within the meaning of 35 U.S.C. § 103(a) to integrate a north bridge on the same integrated circuit chip as video and graphics circuitry. By way of example, while the previous Examiner has performed a search and applicants have also submitted a large number of references related to processing/displaying of video and graphics to the Patent Office, none of these references teach or suggest such integration of north video with video/graphics processing/ displaying circuitry. The absence of any teaching and suggestion for such integration despite its clear advantages of reduced size and reduced potential for system failure, tends to indicate that such integration is not obvious at all.

Therefore, applicants request that the rejection of claim 1 be withdrawn and that it be allowed.

B. Rejection of Claim 2-3, 14, 18-19, 23, 25, and 49

In rejecting claims 2-3, 14, 18-19, 23, 25, and 49, the Office Action states "Sporer discloses the system bridge controller is capable of performing format conversion between big-endian data and little endian data, between the CPU and one or more of the plurality of peripheral devices, between the CPU and at least one of the MPEG video decoder, the means for displaying the video and the other components for processing video and graphics," and cites FIGs. 1-3.

First of all, applicants do not see how "performing format conversion between big-endian and little endian data" is disclosed in FIGs. 1-3.

Further, for similar reasons as claim 1 discussed above, Sporer et al. does not disclose "coupling the CPU to a plurality of peripheral devices via a system bridge controller having a north bridge function on an integrated circuit chip, wherein the integrated circuit chip is used to process MPEG video data" as in claim 22 of the present application, or "[a] system on an integrated circuit chip comprising: an MPEG Transport processor . . . an MPEG video decoder . . . and a system bridge controller" as in claim 41; therefore, Sporer et al. does not anticipate any of claims 1, 22, and 41.

Since claims 2-3, 14, 18-19, 23, 25, and 49 depend, directly or indirectly, from claims 1, 22 and 41, respectively, they incorporate all the terms and limitations of claim 1, 22 or 41 from which they depend in addition to other limitations, which together further patentably distinguish them over the cited references. Therefore, applicants request that the

rejection of claims 2-3, 14, 18-19, 23, 25, and 49 be withdrawn and that they be allowed.

C. Rejection of Claims 5 and 26

In rejecting claims 5 and 26, the Office Action states "Sporer discloses plurality of peripheral devices include one or more PCI devices and wherein the system bridge controller includes a PCI bridge for coupling the CPU to the one or more PCI devices," and cites Col. 7, line 58 to Col. 8, lines 41 of Sporer et al.

As discussed above, Sporer et al. in FIG. 1 unequivocally teaches using the PCI Bridge 34 that is external to the video processing circuit 22. Therefore, Sporer et al. cannot possibly anticipate "a system on an integrated circuit chip comprising: an MPEG video decoder . . . and a system bridge controller" or "a system bridge controller having a north bridge function on an integrated circuit chip . . . used to process MPEG video data," wherein the system bridge controller includes a PCI bridge.

Further, since claims 5 and 26 depend from claims 1 and 22, respectively, they incorporate all the terms and limitations of claim 1 or 22 from which they depend in addition to other limitations, which together further patentably distinguish them over the cited references. Therefore, applicants request that the rejection of claims 5 and 26 be withdrawn and that they be allowed.

D. Rejection of Claims 6, 10, 27 and 31

In rejecting claims 6, 10, 27 and 31, the Office Action states "Sporer discloses the PCI bridge is capable of performing a DMA function between the one or more PCI devices and an external memory." As these claims depend, directly or indirectly, from claims 1 and 22, respectively, they incorporate all the terms and limitations of claim 1 or 22 from which they depend, in addition to other limitations which together further patentably distinguish them over the cited references. Therefore, applicants request that the rejection of claims 6, 10, 27 and 31 be withdrawn and that they be allowed.

E. Rejection of Claims 7-8, 12-13, 28-29, 33-34, and 37-38

The Office Action states "Sporer discloses PCI bridge is capable of performing format conversion between big/little endian data used in the CPU and little/big endian data used in the one or more PCI devices," and cites col. 1, line 52 to col. 2, line 9 and col. 7, line 58 to col. 10, line 67. After having reviewed this vast range of text in the specification, applicants do not see any disclosure of such big/little endian format conversion.

Further, since claims 7-8, 12-13, 28-29, 33-34 and 37-38 depend, directly or indirectly, from claims 1 and 22, respectively, they incorporate all the terms and limitations of claim 1 or 22 from which they depend, in addition to other limitations which together further patentably distinguish them over the cited references. Therefore, applicants request that the rejection of claims 7-8, 12-13, 28-29, 33-34 and 37-38 be withdrawn and that they be allowed.

F. Rejection of Claims 9, 11, 16, 17, 30, 32, 35, 36 and 50-51

Claims 9, 11, 16, 17, 30, 32, 35, 36 and 50-51 have been rejected on various different grounds as allegedly being anticipated by Sporer et al. Since claims 9, 11, 16, 17, 30, 32, 35, 36 and 50-51 depend, directly or indirectly, from claims 1, 22 and 41, respectively, they incorporate all the terms and limitations of claim 1, 22 or 41, in addition to other limitations which together further patentably distinguish them over the cited references. Therefore, applicants request that the rejection of claims 9, 11, 16, 17, 30, 32, 35, 36 and 50-51 be withdrawn and that they be allowed.

G. Rejection of Claims 22 and 41

As discussed above, Sporer et al. does not disclose "coupling the CPU to a plurality of peripheral devices via a system bridge controller having a north bridge function on an integrated circuit chip, wherein the integrated circuit chip is used to process MPEG video data" as in claim 22 of the present application, or "[a] system on an integrated circuit chip comprising: an MPEG Transport processor . . . an MPEG video decoder . . . and a system bridge controller" as in claim 41; hence, Sporer et al. does not anticipate claims 22 and 41. Further, for reasons similar to those given in reference to FIG. 1, claims 22 and 41 are not obvious in view of the art of record. Therefore, applicants request that the rejection of claims 22 and 41 be withdrawn and that they be allowed.

H. Rejection of Claims 15, 20-21, 24, 39, 42, 46 and 48

Claims 15, 20-21, 24, 39, 42, 46 and 48 appear to have been rejected based on the same or similar grounds as claims 1, 22 and 41, respectively. Since claims 15, 20-21, 24, 39, 42, 46 and 48 depend from claims 1, 22 and 41, respectively, they incorporate all the terms and limitations of claim 1, 22 or 41 in addition to other limitations, which together further patentably distinguish them over the cited references. Therefore, applicants request that the rejection of claims 15, 20-21, 24, 39, 42, 46 and 48 be withdrawn and that they be allowed.

In view of the foregoing arguments, applicants respectfully request that the rejection of claims 1-3, 5-39, 41, 42, 46 and 48-51 be withdrawn and that they be allowed. If there are any remaining issues that can be addressed over the telephone, the Examiner is invited to call applicants' attorney at the number listed below.

Respectfully submitted,
CHRISTIE, PARKER & HALE, LLP

By _____
Jun-Young E. Jeon
Reg. No. 43,693
626/795-9900

JEJ/vdw
VDW PAS588428.1-*-10/12/04 10:30 AM